Radiation tolerance of a 0.13µm commercial CMOS technology

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Introduction

- With our resources, long cycles from early development to technology use
- Technologies are getting more complicated… and expensive
- Need to start ahead of time, and group more users

Cycle for quarter micron

1996	First discussions and measurements
1997	Proposal RD49 “Radtol”, measurements on 5 technologies
1998	First design: “DEEP1”
1999	First MPW1
2000	First dedicated engineering runs

Outline

- Technology choice
- Test structures
- TID results
- SEE results
- Conclusion (for the time being…)

Technology choice

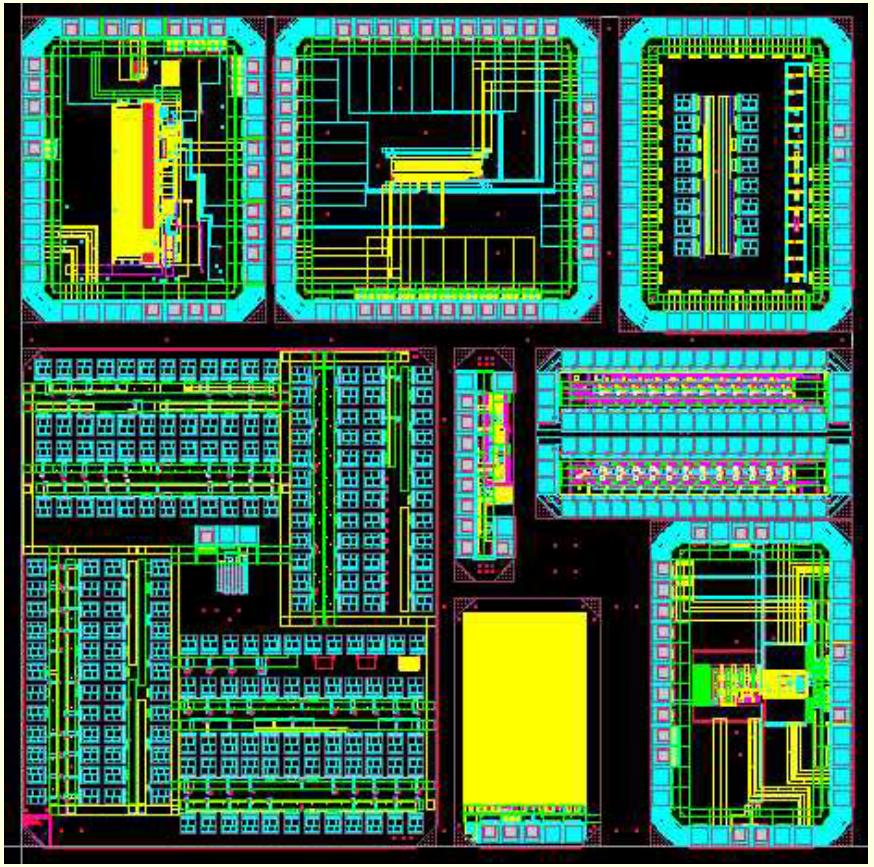
- Skip 0.18μm – already peak production
- Next wave: 0.13μm technology node
- Features of the chosen technology:
  - All-copper technology
  - Vdd=1.2-1.5 V
  - Triple gate oxide
  - Min lithographic image 0.11μm
  - 4 to 8 metal levels (options on stack)
  - Planarization and interlevel dielectrics with low-k
- Device options:
  - Standard, High and Low Vt NMOS and PMOS, ZeroVt NMOS
  - Ultra-thin gate oxide NMOS and PMOS
  - Thick oxide (2.5 V) NMOS and PMOS, ZeroVt NMOS
  - n+, p+ and pc resistors
  - Metal-Metal capacitors

Test structures

- Wafer with macros from foundry (received 1/02, hardware 01)
- SRAM from foundry for SEEs (received 10/01)
- Design of 5x5 mm^2 module in Foundry MPW, with RAL and Imperial College (submitted 11/02, received 3/03):
  - Individual transistors of all types (enclosed, linear)
  - Individual transistors for noise measurements
  - Resistors & Diodes
  - FoxFETs
  - Shift register for SEEs
  - Circuit building blocks (TDC, Fast serializer for optical digital transmission, bandgap, FEAmplifier, SRAM)

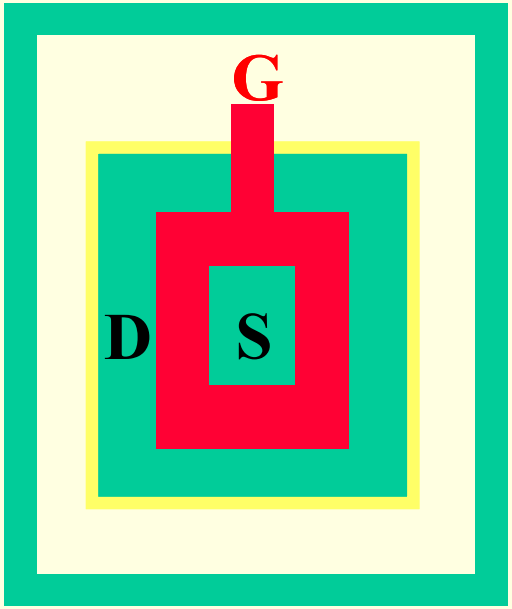
“CuTe1” module

- Run options:
  - 6 levels of metal (4 thin; 2 thick)
  - Mimcap
  - Op resistors
  - All transistors (all Vts, all oxide thicknesses)



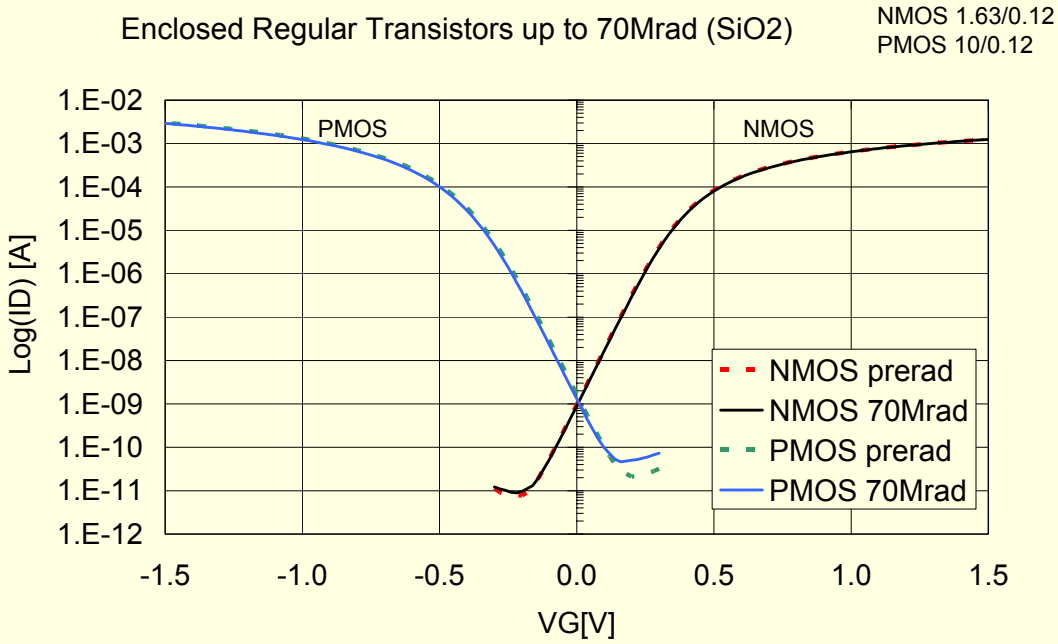
TID results

- Chapters:
  - Enclosed transistors
  - Large linear transistors, W=10μm
  - Narrow linear transistors, minimum W



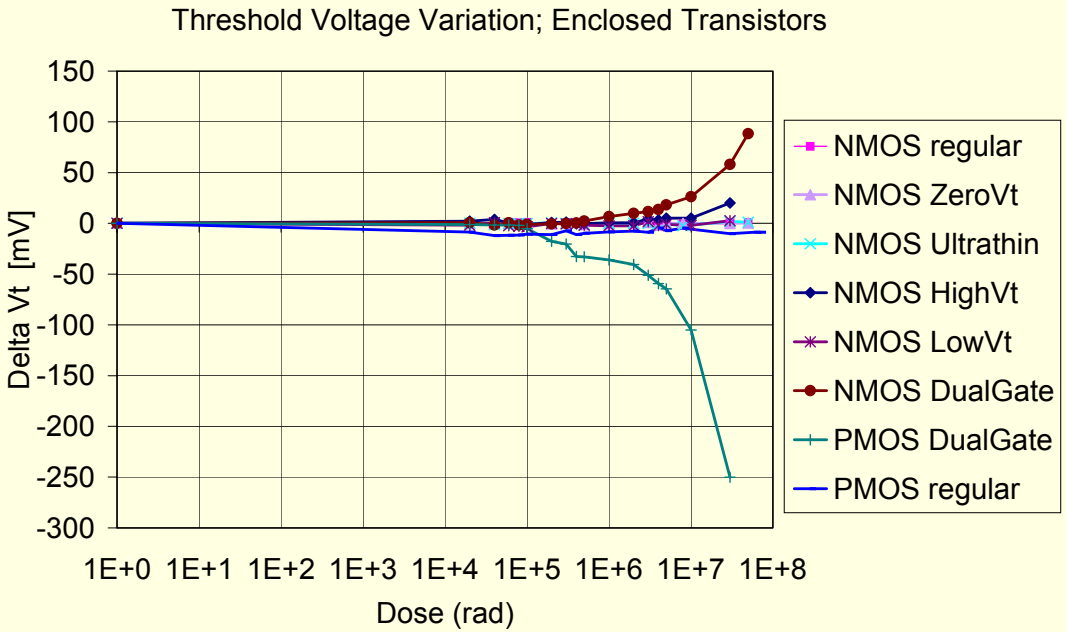
TID results: enclosed transistors

- All TID irradiations with X-rays
- Negligible degradation for all thin-oxide enclosed transistors (NMOS and PMOS), for all parameters



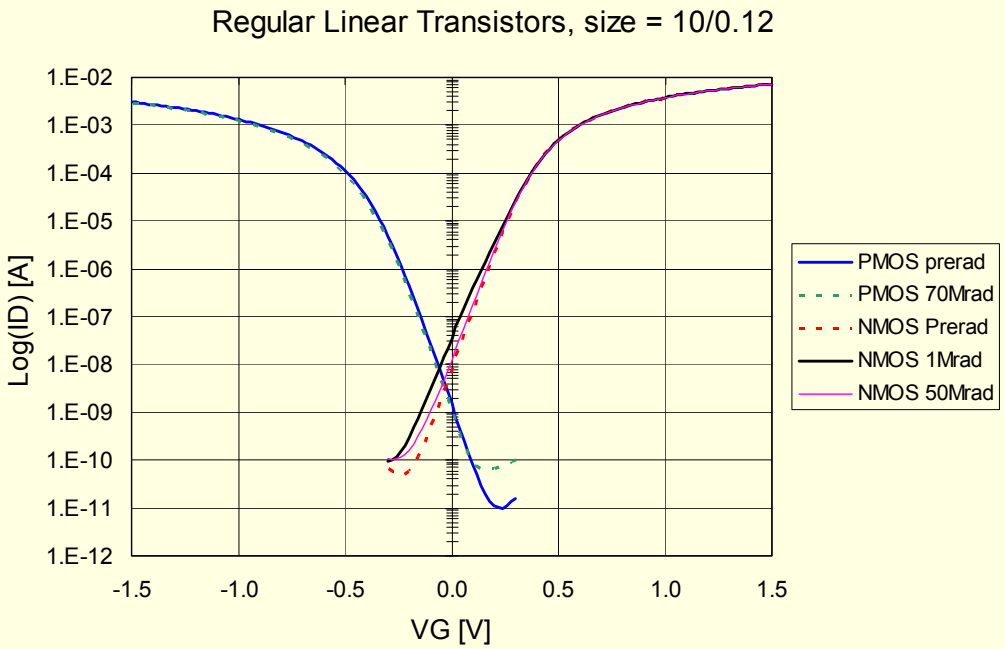
TID results: enclosed transistors

- W=10μm, L = min size:
  - Standard, HighVt, LowVt, Ultrathin = 0.12μm
  - DualGate = 0.26μm; ZeroVt = 0.42μm



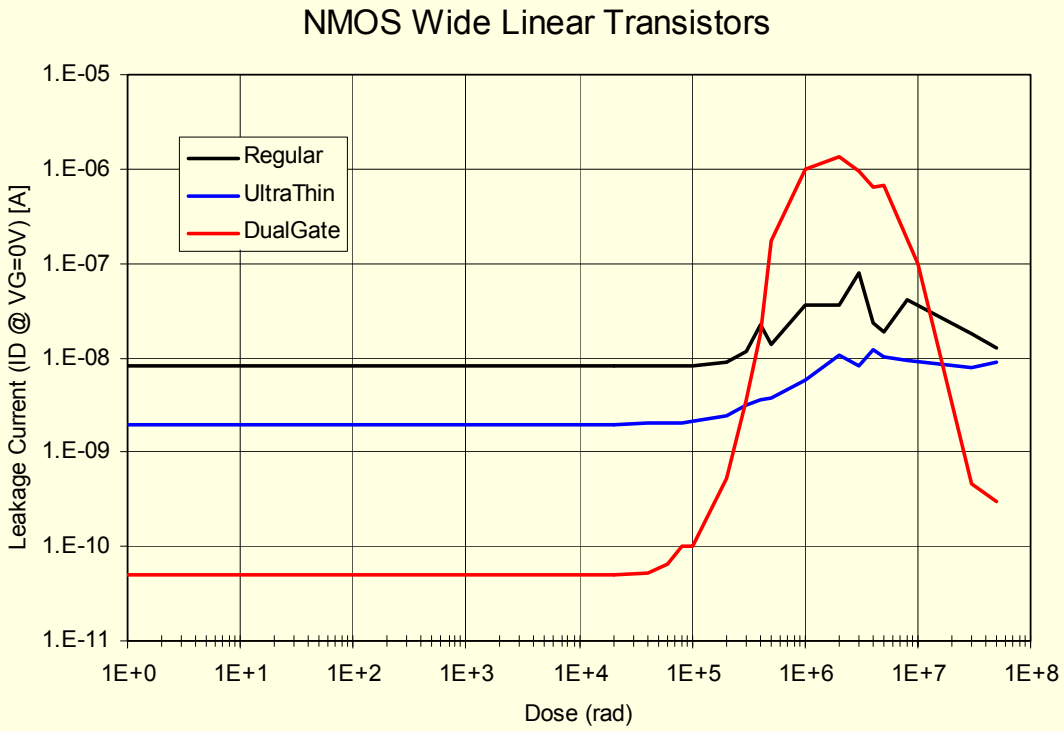
TID results: wide linear transistors

- ΔVt comparable to enclosed transistors
- PMOS overall comparable to enclosed transistors
- NMOS: edge effect (SMALL!!)



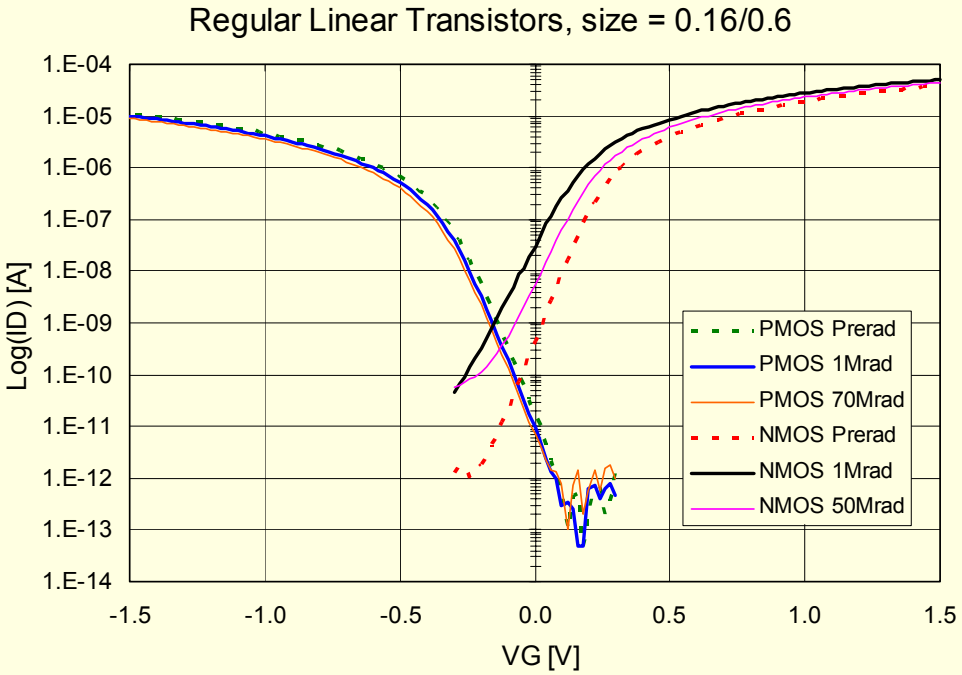
TID results: wide linear transistors

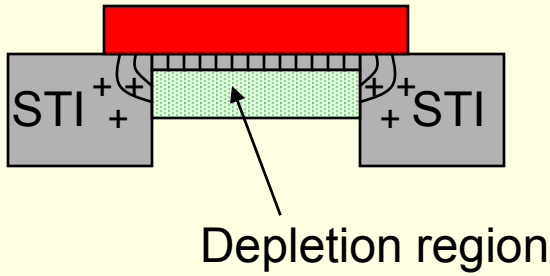
- Leakage current changes with dose: peak at 1-5Mrad



TID results: narrow linear transistors

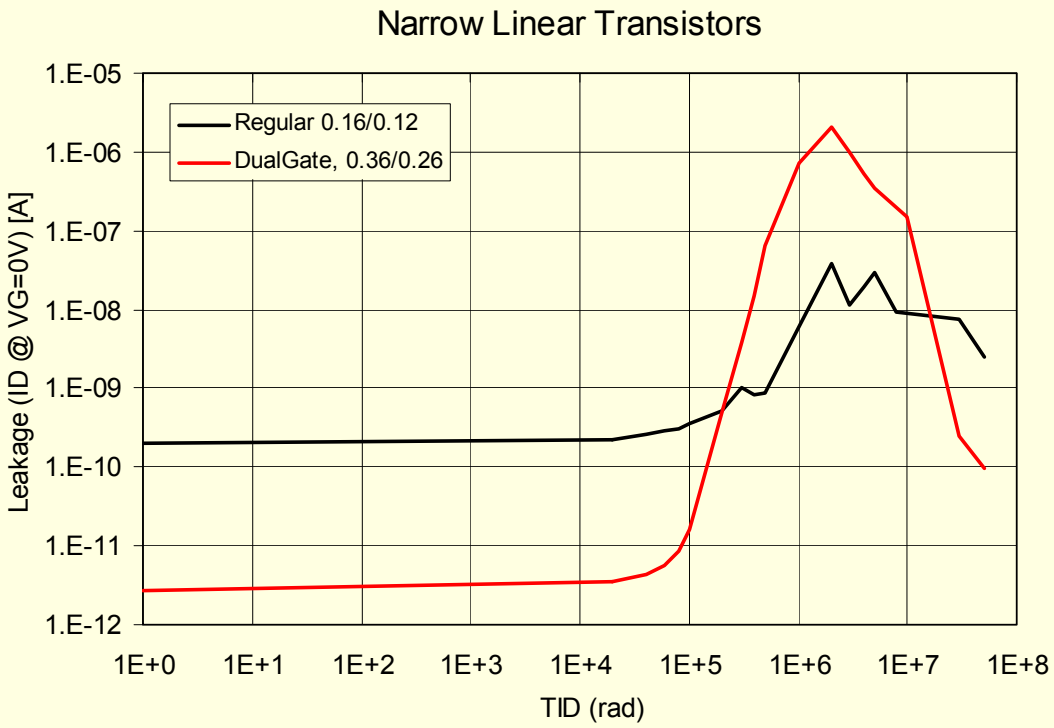
- Change in Vt and subthreshold slope, hence leakage
- Strong edge effect: Narrow Channel Effect
- All transistor types affected





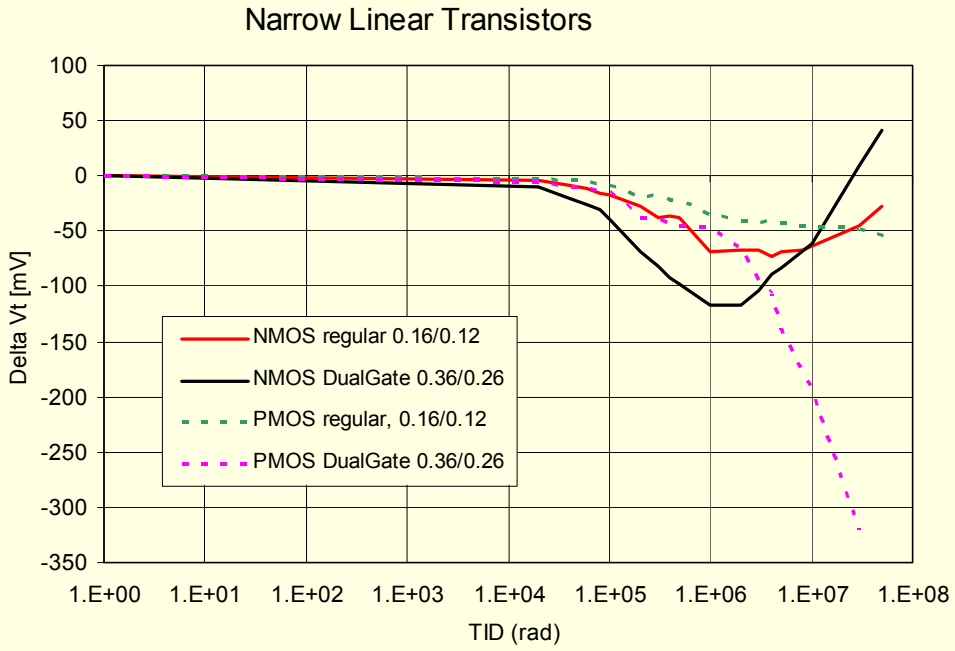
TID results: narrow linear transistors

- Leakage current changes with dose: peak at 1-3Mrad



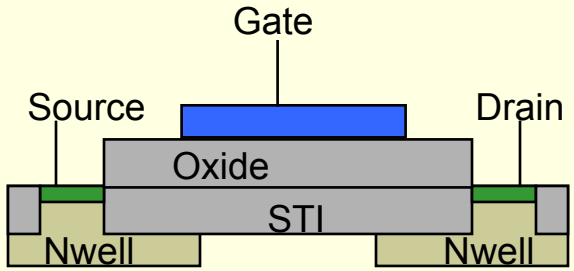
TID results: narrow linear transistors

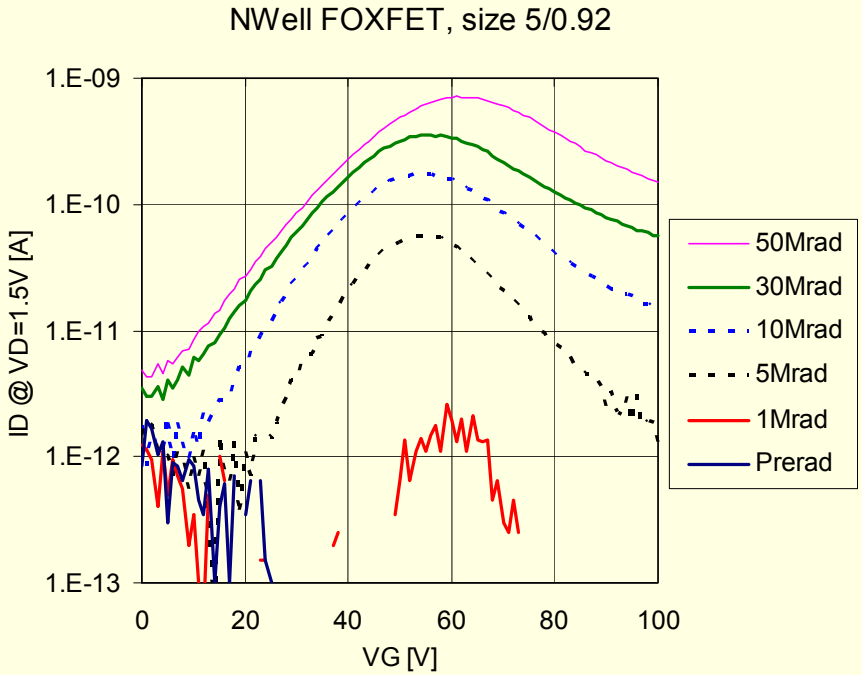
- Threshold voltage shift not negligible – especially for Dual Gate
- Peak in degradation for NMOS at 1-5Mrad



TID results: FOXFETs

- Transistors on Field Oxide
- PC or M1 “gate”
- N+ diffusion or Nwell Source & Drain
- Only Nwell-Nwell has some current (at voltages well above Vdd!)





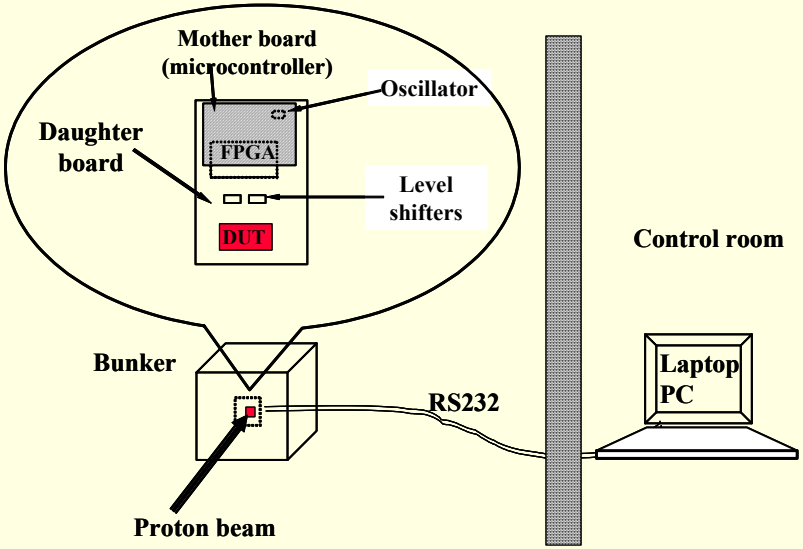
TID results: summary

- Enclosed transistors are very good, as expected (very thin gate oxide)
- DualGate transistors (for I/Os and analog at 2.5V) have to be used carefully – Vt shift is not negligible at high doses
- Large linear transistors look very good also for vast majority of applications
- Narrow linear transistors are more sensitive
- From FOXFETs, lateral isolation is not a problem

- Where is the “border” between narrow and large channels?
- Annealing effects to be studied in more detail

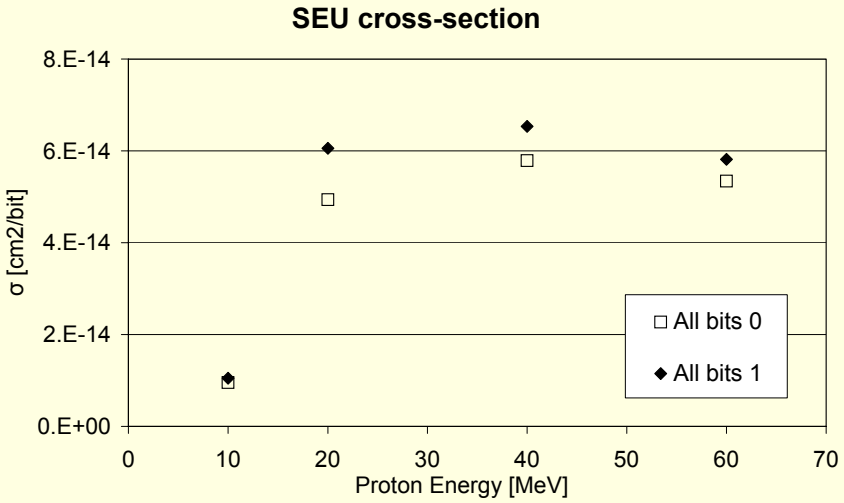
SEEs on SRAM

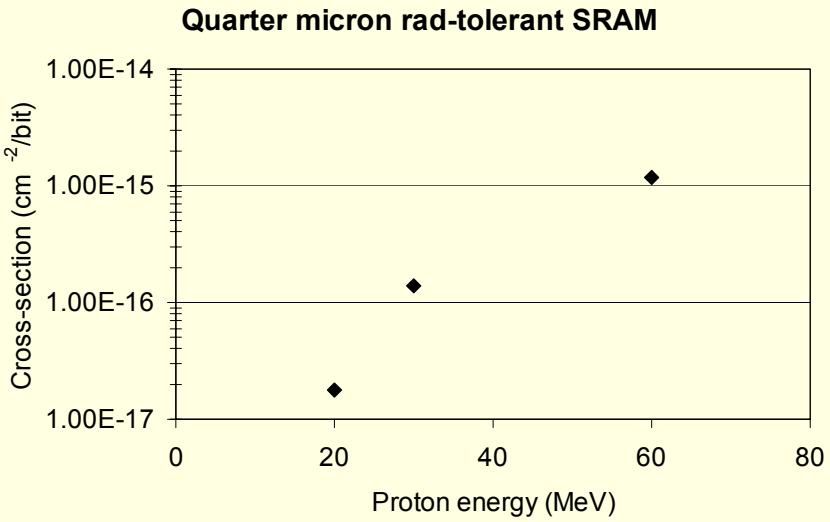
- 16k x 16 SRAM design from Foundry (linear transistors)
- Irradiation at PSI: up to 60MeV protons
- Flux: 1-4x10^8 p/cm^2s
- Proton energy 10, 20, 40 and 60 MeV
- 2 patterns: all-1 and all-0
- SEL detection active at all times
- Vdd = 1.5V and 1.25V



SEEs on SRAM

- Equivalent TID of 260 krad (Si)
- No SEL detected
- σ increases by 20-30% for TID of about 90 krad
- σ increases by 20-30% for lower power supply (1.25V)





Conclusion (for the time being…)

- TID
  - Enclosed transistors are very good
  - No guardring needed
  - Linear transistors look very promising, details still to be studied (annealing, narrow channel effects)
  - DualGate are more sensitive: careful use
- SEEs
  - Sensitive charge smaller, higher SEU sensitivity
  - NB: without enclosed transistors, error rates can be considerably higher than for present 0.25μm designs
  - SEL not observed and not expected to be a crucial issue for our applications (careful: design-dependent sensitivity)